ONE MASK HIGH DENSITY CAPACITOR FOR INTEGRATED CIRCUITS

CROSS-REFERENCE TO RELATED APPLICATIONS

The following co-pending patent applications are related and hereby incorporated by reference:

U. S. Patent Appl. No. (TI-35260), filed _____ to Burke et al.

U. S. Patent Appl. No. (TI-36382), filed _____ to Papa Rao et al.

FIELD OF THE INVENTION

[0001] The invention is generally related to the field of forming capacitors in semiconductor devices and more specifically to forming high density capacitors at the top metal interconnect level.

BACKGROUND OF THE INVENTION

[0002] As semiconductor technology continues to scale, the supply or operating voltage of the integrated circuit becomes lower and lower. The nominal supply voltage has decreased from 5V to 3.3V to 1.8V and below. Transistors with operating voltages of 1.1V are currently being developed.

[0003] As the supply voltage decreases it becomes increasingly important to limit the voltage swing on the supply voltage lines. This is due to the fact that smaller voltage swings can cause unacceptable amounts of current leakage and even unintentionally switch the state of the transistor. Voltage swing may be minimized by providing capacitance on the power supply. Typically this is accomplished with off-

chip decoupling capacitors. As the amount of voltage swing that can be tolerated is reduced, more and more decoupling capacitance is required.

SUMMARY OF THE INVENTION

[0004] The invention is an on-chip decoupling capacitor and method of fabrication. The decoupling capacitor is integrated at the top metal interconnect level and may be implemented with only one additional masking layer.

[0005] An advantage of the invention is providing on-chip decoupling capacitance.

[0006] This and other advantages will be apparent to those of ordinary skill in the art having reference to the specification in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] In the drawings:

[0008] FIG. 1 is a cross-sectional diagram of a high density capacitor according to an embodiment of the invention.

[0009] FIGs. 2A-2G are cross-sectional diagrams of the high density capacitor of FIG. 1 at various stages of fabrication.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0010] The invention will now be described in conjunction with copper damascene process utilizing an aluminum cap layer. Those of ordinary skill in the art will appreciate that the benefits of the invention can be applied to other metal interconnect processes.

[0011] As semiconductor devices continue to scale, the decoupling capacitance requirements increase significantly. The parasitic resistance of off-chip capacitance can result in performance penalties. Placing the decoupling capacitors on-chip can reduce or even avoid these performance penalties. However, integrating the decoupling capacitors on-chip can cause other concerns. For example, using a gate oxide capacitor (in which a MOSFET gate oxide layer is also used as the capacitor dielectric) consumes active area. There are also leakage concerns with gate oxide capacitors. Adding a capacitor between contact and M1 (the first level of metal interconnect) adds a mask, may require routing restrictions above the capacitor and causes planarity and thermal budget concerns. Adding a capacitor between metal interconnect lines also causes planarity and thermal budget concerns.

[0012] To alleviate some of these concerns, the preferred embodiment of the invention incorporates a high density capacitor at the top metal interconnect level. The top metal interconnect level is generally used for routing power and ground lines. As such, the interconnect routing is not as dense as the lower metal interconnect levels and there is more space available for forming the decoupling capacitors. Furthermore, since it is the uppermost interconnect level, planarity is not as much of a concern. Thermal budget is also less of a concern because there are fewer remaining steps and those steps remaining are generally performed at lower temperatures.

[0013] A preferred embodiment of the invention is shown in FIG. 1. A high density capacitor 106 is formed above the top metal interconnect 104 between the top metal interconnect 104 and the aluminum cap layer 118. Aluminum cap layer 118 provides a bonding surface which offers better adhesion for ball bonds, bond wires, etc. than copper. Bonding typically occurs during packaging of the integrated circuit to provide connection to the semiconductor device. So, while the aluminum cap layer is metal, it is not considered a metal interconnect level, but merely a capping layer to provide better connection during packaging to the top metal interconnect level 104.

[0014] Top metal interconnect level 104 is formed over semiconductor body 102. Semiconductor body 102 comprises a semiconductor substrate, transistors and other devices, as well as other metal interconnect levels. Only the top metal interconnect level 104 is shown for simplicity. In this embodiment, the top metal interconnect level 104 comprises copper interconnect lines 104a, 104b with appropriate barrier layers.

[0015] High density capacitor 106 comprises a bottom electrode 108, capacitor dielectric 110, and top electrode 112. The top 112 and bottom 108 electrodes comprise an electrically conductive material. In the preferred embodiment, TaN is used. TaN is often used as a barrier in copper interconnects and offers good compatibility with copper processes. Other electrically conductive materials, such as TiN, Ir, Ru, Ta and sandwiches/multi-layer combinations thereof may alternatively be used. Although TaN is used for both the top and bottom electrodes in the preferred embodiment, different materials may in fact be used for the top and bottom electrodes. The capacitor dielectric 110 preferably comprises a high dielectric constant dielectric. In the preferred embodiment, tantalum-oxide is used. Other high-k dielectrics such as hafnium oxide may alternatively be used. While high-k dielectrics are preferred, less high-k materials such as SiN can alternatively be used.

[0016] The high density capacitor 106 is located over first copper interconnect line 104a such that first copper interconnect line 104a is electrically connected to the bottom electrode 108. Connection to the top electrode 112 is made via aluminum cap layer 118. A portion of the aluminum cap layer 118 is electrically connected between the top electrode 112 and a second copper interconnect line 104b. So, for example, first copper interconnect line 104a may be designed as power supply line for which capacitive decoupling is desired and second copper interconnect line 104b may be designed as a ground line.

[0017] A method for fabricating the decoupling capacitor of FIG. 1 will now be discussed with reference to FIGs. 2A -2G. A semiconductor body 102 is processed through the formation of top metal interconnect level 104, as shown in FIG. 2A. Semiconductor body 102 comprises a semiconductor (e.g., silicon) substrate, transistors, and other devices as well as one or more metal interconnect levels. Only the top metal interconnect level 104 is shown for simplicity. The top metal interconnect level 104 may be formed by depositing an etchstop layer 122 (e.g., SiN or SiC), depositing a low-k dielectric layer 124 (e.g., organo-silicate glass or fluorine-doped silicon-oxide glass) and depositing an optional hardmask 126. A trench is etched in the low-k dielectric layer 124 and then a barrier layer (e.g., Ta/TaN) and copper seed layer are deposited over the surface. Copper ECD (electro-chemical deposition) may then be used to overfill the trench with copper. Finally, copper CMP (chemical-mechanical polish) is performed to planarize the surface and remove the excess copper and barrier materials, resulting in the structure of FIG. 2A.

[0018] Referring to FIG. 2B, a bottom electrode material 108 is deposited over the surface of metal interconnect level 104. Bottom electrode material 108 comprises an electrically conductive material. Preferably, bottom electrode material 108 comprises a material that also acts as a diffusion barrier to copper

to prevent copper from diffusing out from copper interconnect lines 104a, 104b. In the preferred embodiment, bottom electrode material 108 comprises TaN. Suitable materials include TaN, TiN, Ir, Ru, Ta, and sandwiches/multi-layer combinations thereof. For example, instead of entirely comprising a copper diffusion barrier, the bottom electrode may instead comprise bilayers in which only one of the layers comprises a copper diffusion barrier. Specifically, the bottom electrode may comprise a TaN layer with a TiN layer as the dielectric interface.

[0019] Next, a capacitor dielectric 110 is formed over bottom electrode layer 108. Preferably, capacitor dielectric 110 comprises a high dielectric constant material such as tantalum-oxide. A high dielectric constant material allows for a larger capacitance value to be formed in a smaller area. Other high-k dielectric materials such as hafnium oxide or less high-k dielectrics such as SiN may alternatively be used. In the preferred embodiment, a layer of tantalum-oxide 130 is deposited over bottom electrode material 108, as shown in FIG. 2B. The layer of tantalum-oxide130 is then annealed in O_2 to reduce impurities in the tantalum-oxide 130 and increase the oxygen content, thus forming the capacitor dielectric 110 in FIG. 2C.

[0020] Still referring to FIG. 2C, the top electrode material 112 is deposited over the capacitor dielectric 110. The top electrode material 112 comprises an electrically conductive material and may comprise the same or a different material than bottom electrode material 108. In the preferred embodiment, top electrode material 112 comprises TaN.

[0021] Next, a pattern 132 is formed over top electrode material 112, as shown in FIG. 2D. Pattern 132 covers the area where decoupling capacitors are desired. Top electrode material 112, capacitor dielectric 110, and bottom electrode material 108 are then etched, using pattern 132 to create high density capacitor

106. An etch that can etch the bottom electrode selectively with respect to the copper of copper interconnect liner 104b should be selected. For example, the etch chemistry may comprise fluorocarbon and argon gas mixtures. Pattern 132 is then removed.

[0022] Referring to FIG. 2E, the protective overcoat 116 is deposited. In the preferred embodiment, a layer of SiN 114 is first deposited over the surface followed by the deposition of the protective overcoat 116. For example, protective overcoat 116 may comprise a silicon-oxynitride or oxide layer. Protective overcoat 116 and SiN 114 are then patterned and etched to expose a portion of copper interconnect line 104b and a portion of top electrode 114 as well as all other areas of the device where external connections are desired (i.e., bondpad areas).

[0023] Referring to Fig. 2F, a metal capping layer 118 is deposited over the structure. Typically, metal capping layer 118 comprises aluminum to improve adhesion of the bond wires typically applied during packaging. Metal capping layer 118 is patterned and etched to provide individual caps (i.e., unconnected) for each bondpad, as is known in the art. However, where decoupling capacitors are placed, metal capping layer 118 connects between the top electrode 112 and a neighboring copper interconnect line 104b. FIG. 2G, shows a third copper interconnect line 104c having a standard metal cap 134.

[0024] Processing then continues to package the semiconductor devices. During packaging, ball bonds and other bonding methods are used to connect the bondpads of a semiconductor device to the external pins of the integrated circuit.

[0025] While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well

as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.